IN THE CLAIMS:

Claim 1. (Currently amended) An integrated circuit test device comprising:

a substrate having an integrated circuit thereon and including interconnects formed by an internal metallization layer ~~and interconnecting integrated circuit devices~~;

a plurality of bond pads formed ~~above the~~ about an outer region of said substrate; and

a ~~first~~ conductive trace formed by ~~the~~ said internal metallization layer ~~at an outer region of the substrate~~ and coupled to at least two of ~~the~~ said plurality of bond pads, ~~the first~~ said conductive trace and said at least two of said plurality of bond pads electrically isolated from ~~the~~ said integrated circuit and said interconnects.

Claim 2. (Currently amended) The integrated circuit test device of Claim 1 wherein ~~the first isolated~~ said conductive trace surrounds ~~a~~ said plurality of bond pads.

Claim 3. (Currently amended) The integrated circuit test device of Claim 2 wherein ~~the first isolated~~ said conductive trace has a chamfered region.

Claim 4. (Canceled)

Claim 5. (Currently amended) The integrated circuit test device of Claim 1 further comprising at least two separate ~~wherein the first isolated~~ conductive traces ~~trace comprises at least two separate first isolated conductive traces~~.

Claim 6. (Currently amended) The integrated circuit test device according to Claim 5 wherein ~~the~~ said at least two separate ~~first isolated~~ conductive traces have a varying height relative to an upper surface of ~~the~~ said substrate.

Claim 7. (Currently amended) The integrated circuit test device according to Claim 1 wherein ~~the first isolated~~ said conductive trace is formed at the periphery of ~~the~~ said integrated circuit.

Claim 8. (Currently amended) The integrated circuit test device of Claim 1 further comprising ~~wherein the first isolated conductive trace comprises~~ at least two separate isolated conductive traces, each of ~~the~~ said separate isolated conductive traces coupled to at least two of ~~the~~ said plurality of bond pads.

Claim 9. (Canceled)

Claim 10. (Currently amended) An integrated circuit test device comprising:

a substrate having an integrated circuit thereon and including interconnects formed by an internal metallization layer ~~and interconnecting integrated circuit devices~~;

a plurality of bond pads formed ~~above the~~ about an outer region of said substrate; and

a conductive ~~tester runner~~ test circuit on said substrate consisting of ~~formed by the~~ a conductive trace formed by said internal metallization layer ~~and around the plurality of bond pads~~ and electrically coupled to at least two of ~~the~~ said plurality of bond pads, ~~the~~ said conductive test

circuit ~~tester runner and at least two bond pads~~ electrically isolated from ~~the~~ said integrated circuit and said interconnects.

Claim11. (Currently amended) The integrated circuit test device of Claim 10 further comprising a plurality of conductive traces ~~isolated conductive tester runners~~.

Claim12. (Currently amended) The integrated circuit test device according to Claim 11 wherein at least two of ~~the~~ said plurality of ~~the isolated conductive tester runners having~~ conductive traces have a varying height relative to an upper surface of ~~the~~ said substrate.

Claim 13. (Currently amended) The integrated circuit test device of Claim 10 wherein ~~the isolated~~ said conductive trace ~~tester runner~~ has a chamfered region.

Claims 14-15 (Canceled)